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Economical Approach for Power Quality Improving in Multi Feeder Distribution Systems Using Interline DVR

Dr. P.Vasudeva Naidu*

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PCC.

Abstract:

This paper deals with economical approach for power quality improving in multi feeder distribution system using interline converter custom power devices (I-CPDs) such as Interline dynamic voltage restorer (I-DVR). The main aim of this CPDs is required exchange real power from healthy feeder to faulty feeder in distribution system using common DC-link. This paper discussed the modeling of I-DVR and selection of capacitor rating and mitigate the power quality problems in multifeeder distribution systems. Simulation of the distribution system model is verified with MATLAB/Simulink to validate the proposed system.

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Author correspondence:

Dr.P. Vasudeva Naidu,
Asst.Professor, EEE Dept, GITAM (deemed to be University), Hyderabad, India.
Corresponding Author Email Id: pvdnaidu81@gmail.com

I. INRODUCTION

Now a days, because of large use of power electronic devices such as uninterrupted power supplies, adjustable speed drives etc., in distribution systems, the power quality problems are very important. The most regular power quality situations are flicker, harmonics, and voltage fluctuations and so on. With today's development towards deregulation and competition between utilities, The present issue of power quality are important. Therefore custom power devices are used to improve power quality. The concept of custom power is first explained by Hingorani [1] in 1955. In order to overcome the disadvantages caused by placing a shunt capacitor in line, facts devices have been developed to solve the problem effectively examples of FACTS devices are SC, TSC...etc. A series connected converter based mitigation device, the Dynamic Voltage Restorer (DVR) [1], is the most economic and technically advanced mitigation device proposed to protect sensitive loads from voltages sags. The DVR injects three single-phase voltages in series with incoming supply voltages. The magnitude and phase angle of injected voltage are variables which result in variable real and reactive power exchange between the DVR and the sensitive load or the distribution system. The amount of

real and reactive power supplied by the DVR depend on the type of voltage disturbance, the protected load and the magnitude and direction of injected voltage. The reactive power can be internally generated within the DVR while an energy storage is required to supply the real power. Thus the amount of energy storage within the DVR becomes one of the main limiting factors in mitigating long duration voltage sags. Therefore researchers presently pay greater attention on the DVR energy storage and its optimum use. A new circuit topology in which the DVR energy storage is dynamically replenished by means of front-end controllable rectifier has been proposed in [2]. A progressive phase advance technique where all the three-phase voltages are progressively advanced by a certain angle α to minimize the amount of real power supplied by the DVR has been proposed in [3]-[4].

This paper presents a concept of inter-line dynamic voltage restoration (IDVR) where two or more voltage restorers are connected such that they share a common DC-link. This is in a way similar to the interline power flow controller (IPFC) concept which is still under research for the compensation and effective power flow management of multi-line transmission system [5]. In its general form, the IPFC employs a number of inverters with a common DC-link to provide series compensation for a selected line of the transmission system. In a similar way, the IDVR system is formed by using several DVRs protecting sensitive loads in different distribution lines to share a common DC-link energy storage. For an example, two different sensitive loads in an industrial park fed from two different feeders with different voltage levels can be protected from voltage sags by two DVRs employed in individual feeder. DC-links of these two DVRs could be connected to a common link to form anIDVR system. This would cut down the cost of custom power device as sharing a common DC-link reduces the DC-link storage capacity significantly compared to that of a system whose loads are protected by clusters of DVRs with separate energy storages.

II. SYSTEM REPRESENTATION

The Fig.1 shows the basic structure of Interline DVR for three-phase four-wire parallel distribution system with nonlinear and unbalanced load. Here, load on feeder 1is nonlinear and unbalanced and that on feeder 2 is sensitive load. The system consist of common DC link with neutral clamped which provides power to the voltage source inverters to inject the series voltages into the parallel feeder lines. The two series active power filters (SEAPFs) inverter consisting of IGBT switches (S11-S16) and (S21-S26), is used to track the reference voltages to be injected in series with respective feeders.

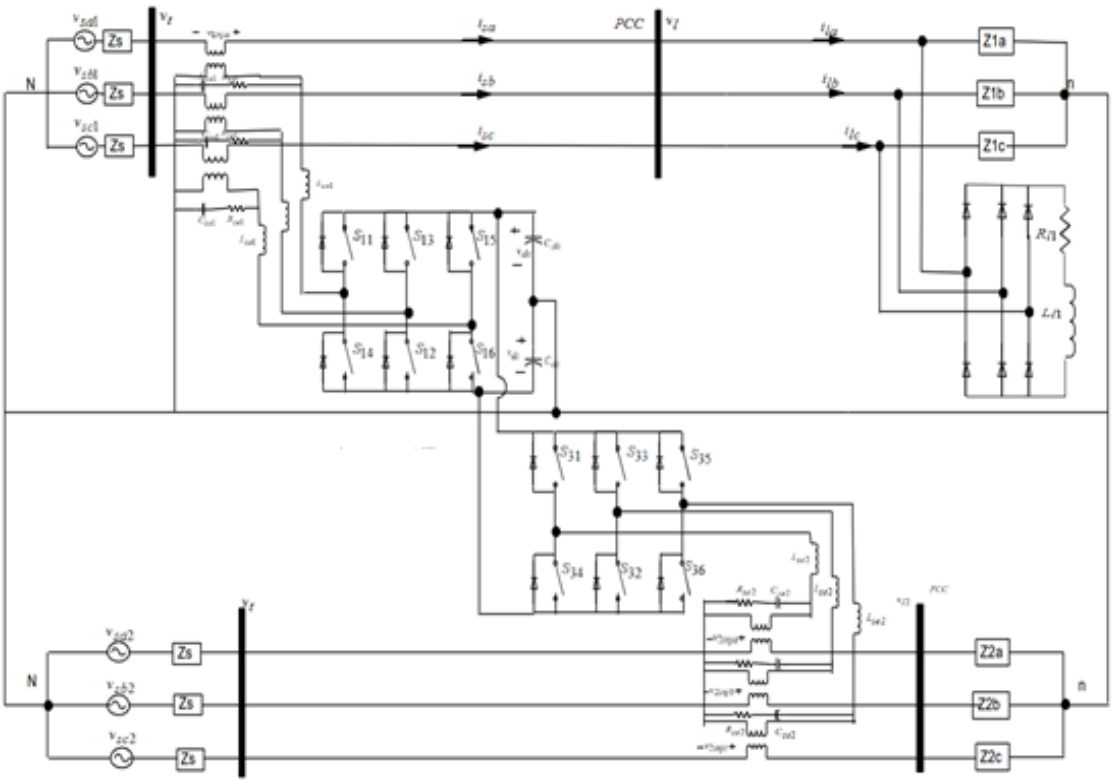


Fig.1.The schematic diagram of a typical interline-DVR in parallel feeder distribution system

2.1 Energy Storage Requirement of a DVR

The injection of an appropriate voltage in the face of up-stream supply voltage sag needs a certain amount of real and reactive power which must be supplied by the DVR. Supply of real power is met by means of an energy storage facility connected in the dc link. Large capacitors are used as a source of energy storage in most of the DVRs. Generally, capacitors are used to generate reactive power in an ac power system. However,in a dc system, capacitors can be used to store energy. When the energy is drawn from the energy storage capacitors, the capacitor terminal voltage decreases. Therefore, there is a minimum voltage (V_{dcmin})below which the inverter of the DVR cannot generate the required voltage. Thus, the size of the dc capacitor needed to supply active powerP_{inj}can be expressed as in (1) interms of maximum allowable dc-link voltage (V_{dcmax}), minmum allowable dc-link voltage (V_{dcmin}), sag duration (T_{sag}),and power loss (P_{loss}). According to (1), it is clear that large capacitors in the dc-link energy storage are needed to effectively mitigate voltage sags of large depths and long durations and power loss (P_{loss}). According to (1), it is clear that large capacitors in the dc-link energy storage are needed to effectively mitigate voltage sags of large depths and long durations.

$$C = \frac{2*(P_{inj} + P_{loss})*T_{sag}}{\left[V_{DC\max}^2 - V_{DC\min}^2\right]} \qquad (1)$$

III. SWITCHING CONTROL

To generate reference injected voltages for I-DVR synchronous reference frame (dqo) theory is used. Here the synchronous reference frame (SRF) theory is used to generate injected voltages for the DVR

in which fault occurs. The block diagram for reference injected voltages required by the DVR is shown in Fig.2.

3.1 HYSTERESIS CONTROLLER

Load voltage regulation in parallel feeder line distribution system by I-DVR with hysteresis voltage controller is presented in this section. This controller compares the actual injected voltages (v_{inj_a},v_{inj_b},v_{inj_c}) by the DVR with the reference generated voltages ($v^*_{inj\_a}$,$v^*_{inj\_b}$,$v^*_{inj\_c}$) by SRF theory with fixed hysteresis band value which varies between 5% to 15% of the rated load voltage. The block diagram of reference injected voltage generation in DVR_1 and hysteresis band controller is show in Fig.2.

3.2 Hysteresis Band Control Switching Logic

The VSI switching (S_{11},S_{13},S_{15}) commands are directly issued to the top switches in legs and their complement signal (S'_{14},S'_{16},S'_{12}) to corresponding bottom switches in legs. The logic of gating signals for switching of inverter is given below,

if $\varepsilon_a \geq +h$, S_{11},= 1, S'_{14}= 0 (S_{11} is ON, $S'_{14}$is OFF)

else if $\varepsilon_a \leq -h$,S_{11},= 0, S'_{14}= 1 (S_{11} is OFF, $S'_{14}$is ON)

end

Similarly the same logic can be applied for other legs of VSI.

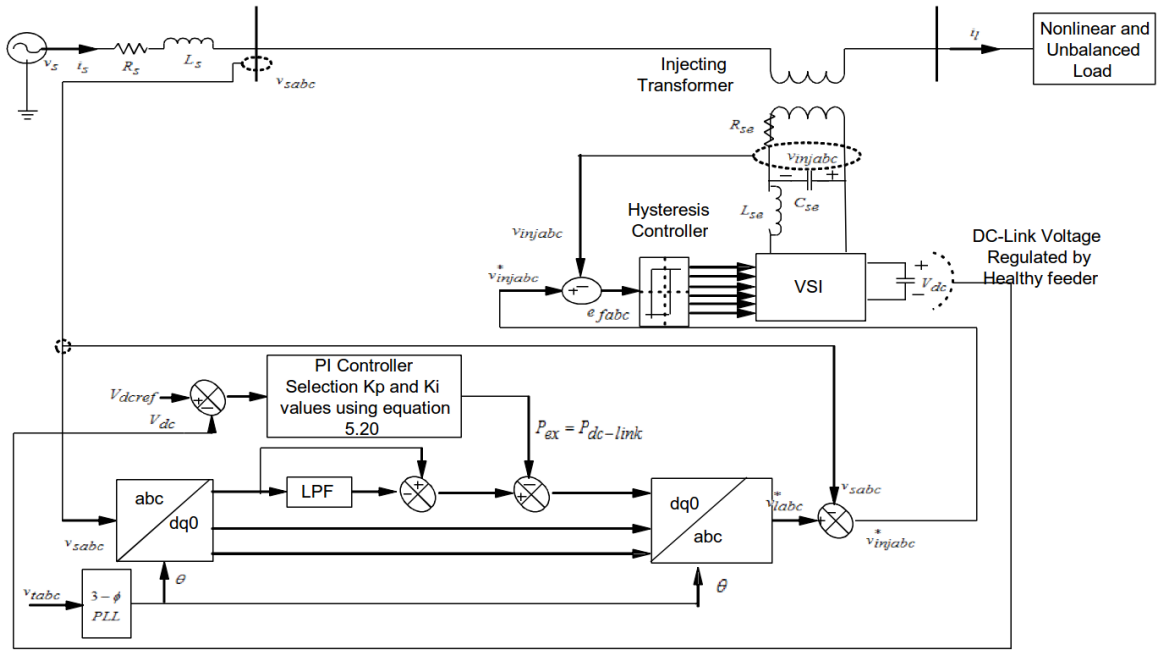


Fig.2 Block diagram of reference injected voltage generation in DVR_1 and hysteresis band controller

IV. RESULTS

The system parameters for the simulation studies for the proposed analysis i.e. SRF Based I-DVR is done by using MATLAB/SIMULINK and shown in Table 1.

Table.1 System Parameters

System Parameters	Values
System voltage and frequency in feeder 1	400 Volts (L-L) rms and 50Hz
System voltage and frequency in feeder 2	400 Volts (L-L) rms and 50Hz
Source impedance on feeder 1	Z_{s1}=1+j0.03141Ω
Source impedance on feeder 2	Z_{s2}=1+j0.03141Ω
Load on feeder 1	Nonlinear Load: Three-Phase bridge rectifier consisting of R-L Load (100Ω and 100mH) Unbalanced load: Z_{la}=150+j31.41Ω, Z_{lb}=75+j31.41Ω, Z_{lc}=50+j3.141Ω,
Load on feeder 2	Unbalanced load: Z_{la}=150+j31.41Ω, Z_{lb}=75+j31.41Ω, Z_{lc}=50+j3.141Ω,
VSC-1 and VSC-2 Series T/F (T_1andT_2)	10Mva,200/200,50Hz, R=0.002 pu, X=0.6 pu
VSC-1 parameters	R_{se1}=1.2Ω, C_{se1}=10 µF and L_{se1} = 15mH
VSC-2 parameters	R_{se1}=1.2Ω, C_{se1}=10 µF and L_{se1} = 15mH
DC Capacitor(C_{DC})	C_{DC1} =2,200µF and C_{DC2} =2,200µF
PI Regulator components	Kp = 0.9938, Ki = 11.5855

4.1 Steady State Analysis

Case 1 - Voltage Sag Occurs on Feeder 1

In this case a sag 30 % with phase-angle jump of -10º is created at feeder 1at time *t= 0.02s* and it is cleared at time *t= 0.04s.*The source voltages and load voltages without I-DVR are shown in Fig. 3 and 4.

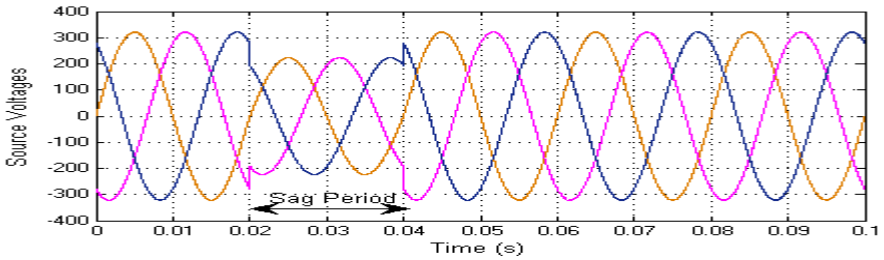


Fig. 3 Three phase source voltages on feeder 1

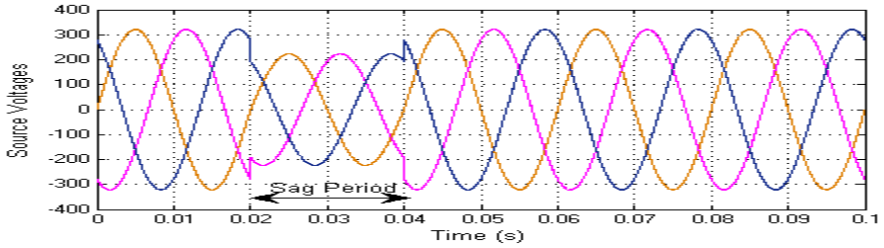


Fig.4 Three phase PCC voltages/Load Voltages on feeder 2

When the compensating device i.e., I-DVR is considered the analysis for same duration of sag is studied. Now the DVR_1 in the feeder-1 is operates by minimum real power injection technique which is explained in chapater-2 and the reference injected voltages required for DVR_1, The waveforms for DVR_1 injected voltages are shown in Fig.5.5.

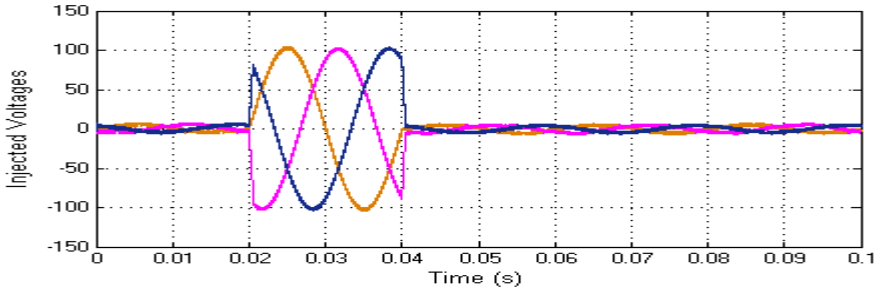


Fig.5.5. Injected Voltages on $SEAPF_1$

At this angle of injection the actual injected voltages tracks the desired reference injected voltages accurately. Here proper selection of voltage controller is required as explained in subsection 5.4. The DC-link voltage is shown in Fig.6. At the period of sag DC link voltage drops, this initial drop is due to the sudden power change in the feeder-1, to nullify this effect the extra power is supplied from the dc-link energy storage as real power controller of feeder-2. This instance takes a certain time to realize the power change, now at feeder 1 DVR_1 injects voltages such that the sag is eliminated and DC-link is brought toward the reference within a short time. Now load voltages are resorted to normal value which are shown in Fig.5.15 and real power (P) exchange at feeder 1 is shown Fig.8. From Fig.7 it is observed that the PCC /load voltages at feeder 1 are perfectly balanced and sinusoidal. The voltages at healthy Feeder 2 remains same even during the period of sag. Which are shown in Fig.5.8 (a) - (c).

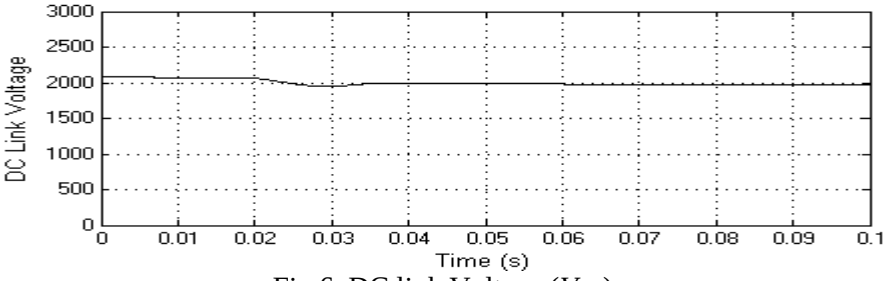


Fig.6. DC link Voltage (V_{DC})

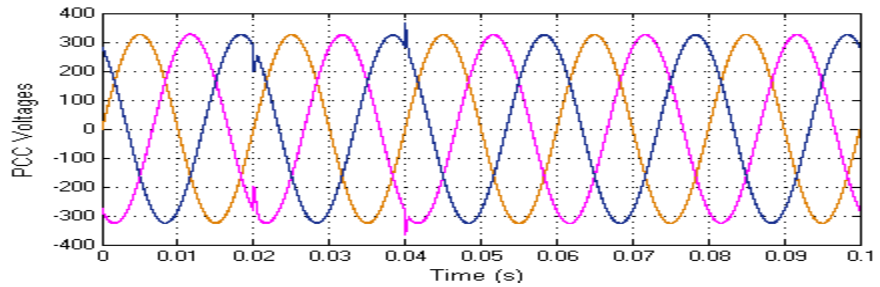


Fig.7. Balanced three phase PCC/load voltages in feeder1

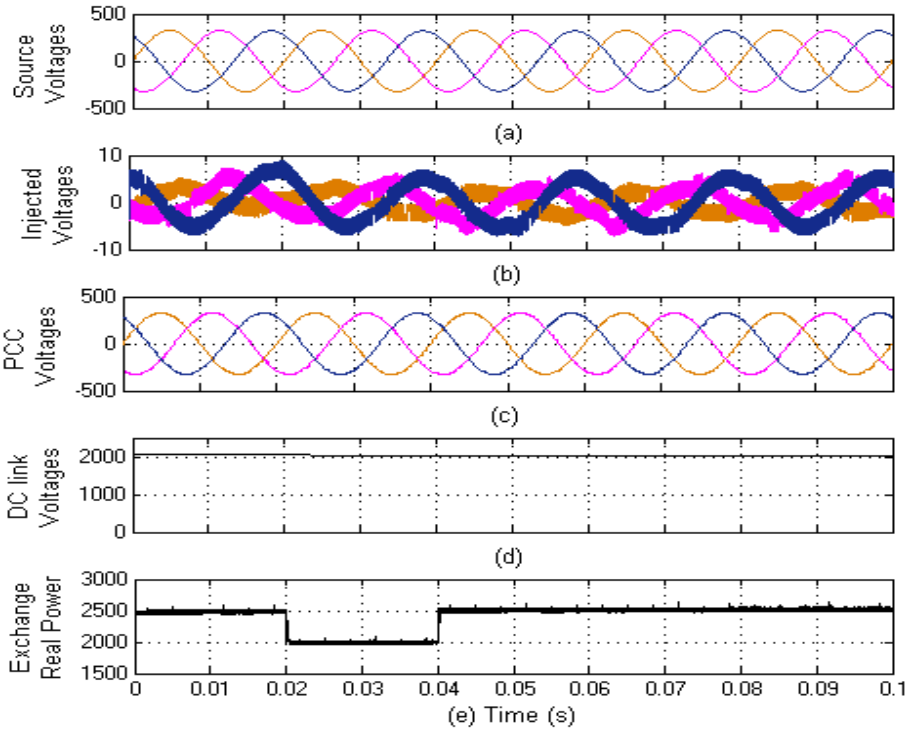
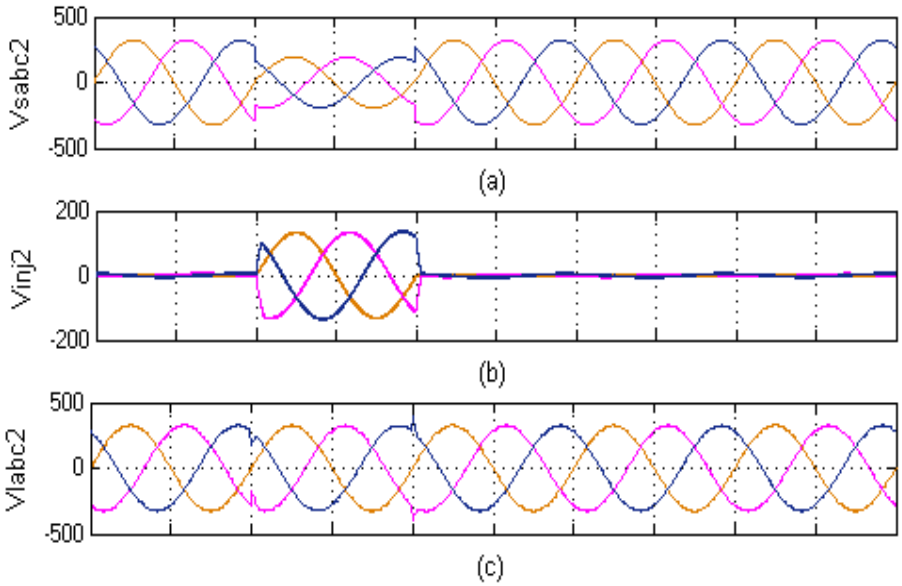
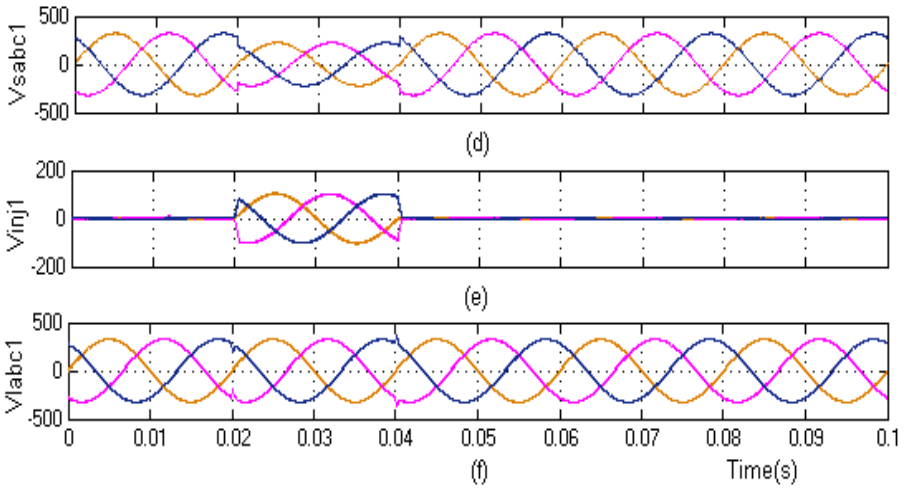


Fig.8.(a) Three phase source voltages at feeder 2, (b) injected voltages of $SEAPF_2$ (c) PCC/load voltages at feeder2, (d) DC link voltage (V_{DC}), (e) exchange real power (P_{ex}).

Case 2 - Voltage sag occurs on both the feeder lines simultaneously at same interval

In this case the different percentage of voltage sag with different phase-angle jumps occurs on both the feeders at same interval of time ($0.02s \leq t \leq 0.04s$) i.e., 30% on feeder 1 and 40% on feeder 2.





V. CONCLUSION

It was also observed that the capacity for power compensation and load voltage regulation of multiline-DVR depends on the rating of the dc storage device. The power quality problems mitigated in multi feeder distribution system using multiline-DVR is presented in this paper and developed for use in Simulink environment with power system block sets. Here a control system is designed in MATLAB Simulink. A multiline DVR can control reactive power and also regulate bus voltages in feeders. It can improve power quality in power system.

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